

MOSTEK®

MDX SERIES™ MICROCOMPUTER SYSTEMS

Operations Manual

MDX-DIOB1 DIGITAL I/O BUS INTERFACE MODULE

MOSTEK MDX-DIOB1
Version 1.0
Operation Manual

TABLE OF CONTENTS

SECTION NUMBER	PARAGRAPH NUMBER	TITLE	PAGE NUMBER
		GENERAL INFORMATION	
1	1.1	FEATURES	1-1
	1.2	MD SERIES GENERAL DESCRIPTION	1-1
2		FUNCTIONAL HARDWARE DESCRIPTION	
	2.1	INTRODUCTION	2-1
	2.2	BLOCK DIAGRAM DESCRIPTION	2-1
3		STRAPPING OPTIONS	
	3.1	ADDRESS CONFIGURATION STRAPPING	3-1
	3.2	MEMORY EXPANSION	3-1
	3.3	ONE WAIT-STATE GENERATOR	3-2
	3.4	<u>BUSAK TO STATUS 0</u>	3-2
	3.5	SHIPPING CONFIGURATION	3-2
4		DIGITAL I/O BUS DESCRIPTION	
	4.1	INTRODUCTION	4-1
	4.2	ADDRESS SIGNALS	4-1
	4.3	CONTROL SIGNALS	4-1
	4.4	DATA SIGNALS	4-2
	4.5	ROUTING	4-2
5		SPECIFICATIONS	
	5.1	ELECTRICAL SPECIFICATIONS	5-1
	5.1.1	WORD SIZE	5-1
	5.1.2	BUS INTERFACE	5-1
	5.1.3	POWER SUPPLY REQUIREMENTS	5-1
	5.1.4	OPERATING TEMPERATURE RANGE	5-1
	5.1.5	INTERRUPTS	5-2
	5.1.6	I/O ADDRESSING	5-2
	5.1.7	I/O CAPACITY	5-2
	5.1.8	SYSTEM CLOCK	5-2

TABLE OF CONTENTS

SECTION NUMBER	PARAGRAPH NUMBER	TITLE	PAGE NUMBER
5 cont.	5.2	MECHANICAL SPECIFICATIONS	5-2
	5.2.1	CARD DIMENSIONS	5-2
	5.2.2	CONNECTORS	5-2
APPENDIX A		SCHEMATIC	A-1
APPENDIX B		PARTS PLACEMENT DIAGRAM	B-1
		PARTS LIST	B-2

LIST OF FIGURES

FIGURE NUMBER	DESCRIPTION	PAGE NUMBER
2-1	BOARD PHOTO WITH OVERLAYS	2-3
2-2	MDX-DIOB1 BLOCK DIAGRAM	2-4
3-1	ADDRESS STRAPPING OPTION WORK SHEET	3-3
4-1	TYPICAL ADDRESS OR CONTROL LINE	4-3
4-2	TYPICAL DATA LINE	4-3

LIST OF TABLES

TABLE NUMBER	DESCRIPTION	PAGE NUMBER
1-1	J1 CONNECTOR PINOUT	1-2
1-2	J2 CONNECTOR PINOUT	1-3
3-1	J3 HEADER PINOUT	3-1

SECTION 1

GENERAL INFORMATION

1.1 FEATURES

- . Provides parallel, memory-mapped DIGITAL I/O BUS.
- . Services up to sixty-four 8-bit I/O ports.
- . Services up to sixteen of MOSTEK's DIOPs.
- . Balanced differential transmission with twisted pair lines.
- . Up to 50 feet DIGITAL I/O BUS length.
- . Address block selectable with jumpers.
- . One wait-state generator option.
- . 4MHz capability.
- . Single +5 volt supply.
- . STD-Z80 BUS compatible.

1.2 MD SERIES GENERAL DESCRIPTION

The MD series and the STD BUS were designed to satisfy the need for low cost OEM microcomputer modules. The STD BUS uses a mother board interconnect system concept and is designed to handle any MD series card type in any slot. The modules for the STD BUS are a compact 4.5 x 6.5 inches which provides for system partitioning by function (RAM, EPROM, I/O). The smaller module size makes system packaging easier while increasing MOS-LSI densities provide high functionality per module.

The MD series of OEM microcomputer boards and the STD BUS offer the most cost effective system configuration available to the OEM system designer.

TABLE 1-1

J1 CONNECTOR PINOUT

	Component Side				Circuit Side			
	PIN	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
Logic Power Bus	1	+5V	In	+5 Volts DC (Bussed)	2	+5	In	+5 Volts DC (Bussed)
	3	GND	In	Digital Ground (Bussed)	4	GND	In	Digital Ground (Bussed)
	5				6			
Data Bus	7	D3	In/Out	Low Order Data Bus	8	D7	In/Out	High Order Data Bus
	9	D2	In/Out	Low Order Data Bus	10	D6	In/Out	High Order Data Bus
	11	D1	In/Out	Low Order Data Bus	12	D5	In/Out	High Order Data Bus
	13	D0	In/Out	Low Order Data Bus	14	D4	In/Out	High Order Data Bus
Address Bus	15	A7	In	Low Order Address Bus	16	A15	In	High Order Address Bus
	17	A6	In	Low Order Address Bus	18	A14	In	High Order Address Bus
	19	A5	In	Low Order Address Bus	20	A13	In	High Order Address Bus
	21	A4	In	Low Order Address Bus	22	A12	In	High Order Address Bus
	23	A3	In	Low Order Address Bus	24	A11	In	High Order Address Bus
	25	A2	In	Low Order Address Bus	26	A10	In	High Order Address Bus
	27	A1	In	Low Order Address Bus	28	A9	In	High Order Address Bus
	29	A0	In	Low Order Address Bus	30	A8	In	High Order Address Bus
Control Bus	31	/WR	In	Write to Port	32	/RD	In	Read from Port
	33				34	/MEMRQ	In	Memory Request
	35				36	/MEMEX	In	Memory Expansion
	37	/REFRESH	In	Dynamic RAM REFRESH	38			
	39				40	/STATUS 0	Out	CPU Status
	41	/BUSAK	In	Bus Acknowledge	42			
	43				44			
	45	/WAITRQ	Out	Wait Request	46			
	47	/SYSRESET	In	System Reset	48			
	49	/CLOCK	In	Clock from Processor	50			
	51				52			
Power Bus	53				54			
	55				56			

All signals are referenced to MDX*DI0B1.

TABLE 1-2

J2 CONNECTOR PINOUT

	PIN	Mnemonic	Signal Flow	Description	Pin	Mnemonic	Signal Flow	Description
Data Bus	1	D7B	In/Out	High Order Data Bit	2	/D7B	In/Out	Inverted High Order Data Bit
	3	D6B	In/Out	High Order Data Bit	4	/D6B	In/Out	Inverted High Order Data Bit
	5	D5B	In/Out	High Order Data Bit	6	/D5B	In/Out	Inverted High Order Data Bit
	7	D4B	In/Out	High Order Data Bit	8	/D4B	In/Out	Inverted High Order Data Bit
	9	D3B	In/Out	Low Order Data Bit	10	/D3B	In/Out	Inverted Low Order Data Bit
	11	D2B	In/Out	Low Order Data Bit	12	/D2B	In/Out	Inverted Low Order Data Bit
	13	D1B	In/Out	Low Order Data Bit	14	/D1B	In/Out	Inverted Low Order Data Bit
	15	D0B	In/Out	Low Order Data Bit	16	/D0B	In/Out	Inverted Low Order Data Bit
Control Bus	17	CRDB	Out	Coded Read	18	/CRDB	Out	Inverted Coded Read
	19	CWRB	Out	Coded Write	20	/CWRB	Out	Inverted Coded Write
Address Bus	21	A5B	Out	Low Order Address Bit	22	/A5B	Out	Inverted Low Order Address Bit
	23	A0B	Out	Low Order Address Bit	24	/A0B	Out	Inverted Low Order Address Bit
	25	A4B	Out	Low Order Address Bit	26	/A4B	Out	Inverted Low Order Address Bit
	27	A3B	Out	Low Order Address Bit	28	/A3B	Out	Inverted Low Order Address Bit
	29	A2B	Out	Low Order Address Bit	30	/A2B	Out	Inverted Low Order Address Bit
	31	A1B	Out	Low Order Address Bit	32	/A1B	Out	Inverted Low Order Address Bit
NOT USED	33				34			
	35				36			
	37				38			
	39				40			

All signals are referenced to MDX-DIOB1.

SECTION 2

FUNCTIONAL HARDWARE DESCRIPTION

2.1 INTRODUCTION

The DIGITAL I/O BUS INTERFACE MODULE, MDX-DIOB1, is a simple interface between the STD-Z80 BUS and MOSTEK's DIGITAL I/O BUS. It provides parallel, memory-mapped I/O to a maximum of sixty-four 8-bit ports. Using 16 of Mostek's DIOPs, MDX-DIOB1 is capable of servicing up to 256 relay modules. A reset signal is encoded onto the DIGITAL I/O BUS so that all MDX-DIOB1 output peripherals can be latched to their off state when a SYSRESET occurs. Figure 2-1 shows a board photo with overlays.

2.2 BLOCK DIAGRAM DESCRIPTION

Figure 2-2 is a block diagram illustrating the flow of address, data, and control signals on the MDX-DIOB1. The three main elements are the address decode, control logic, and differential bus transceivers and drivers. Input and output to the board are provided via one 40-pin connector.

The address decode circuit is used to enable the board by comparing the upper ten address bits to preset strapping options. REFRESH is used in the comparison circuit to disable the board during a refresh cycle. A strapping option to include MEMEX is also provided to allow compatibility with MD systems that use this signal.

The control logic section is used to generate the control signals on the DIGITAL I/O BUS and to enable the data bus transceivers in the proper direction. A one wait-state generator is provided as a strapping option to allow 4MHz operation with extended DIGITAL I/O BUS lengths. All control logic functions are disabled by the address decode circuit with the exception of SYSRESET, which is enabled at all times.

The differential transceiver and driver circuits are used to receive data signals and to transmit address, data, and control signals. Termination resistors are used at the data bus receivers to minimize signal reflections on the DIGITAL I/O BUS.

FIGURE 2-1 BOARD PHOTO WITH OVERLAYS

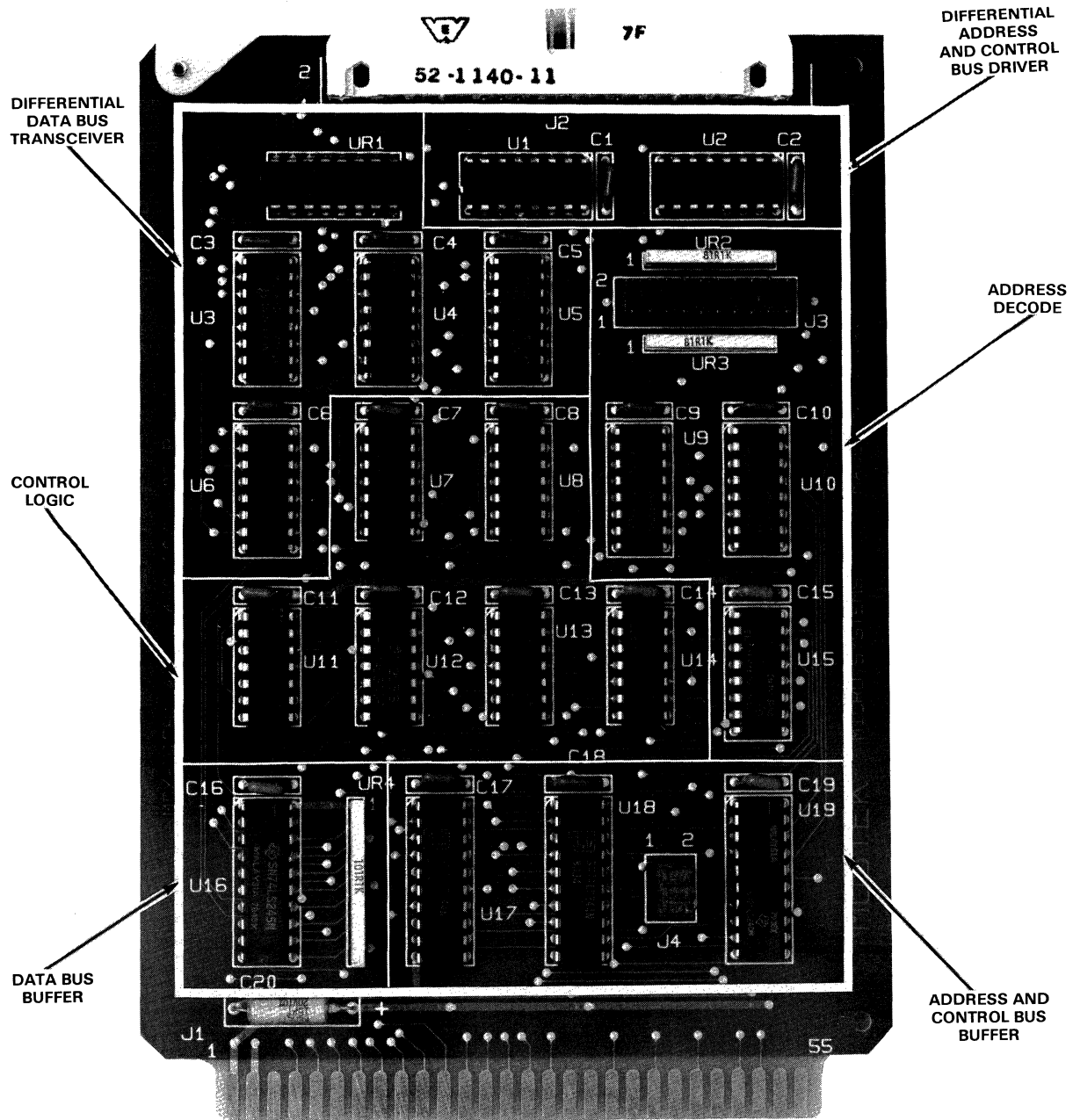
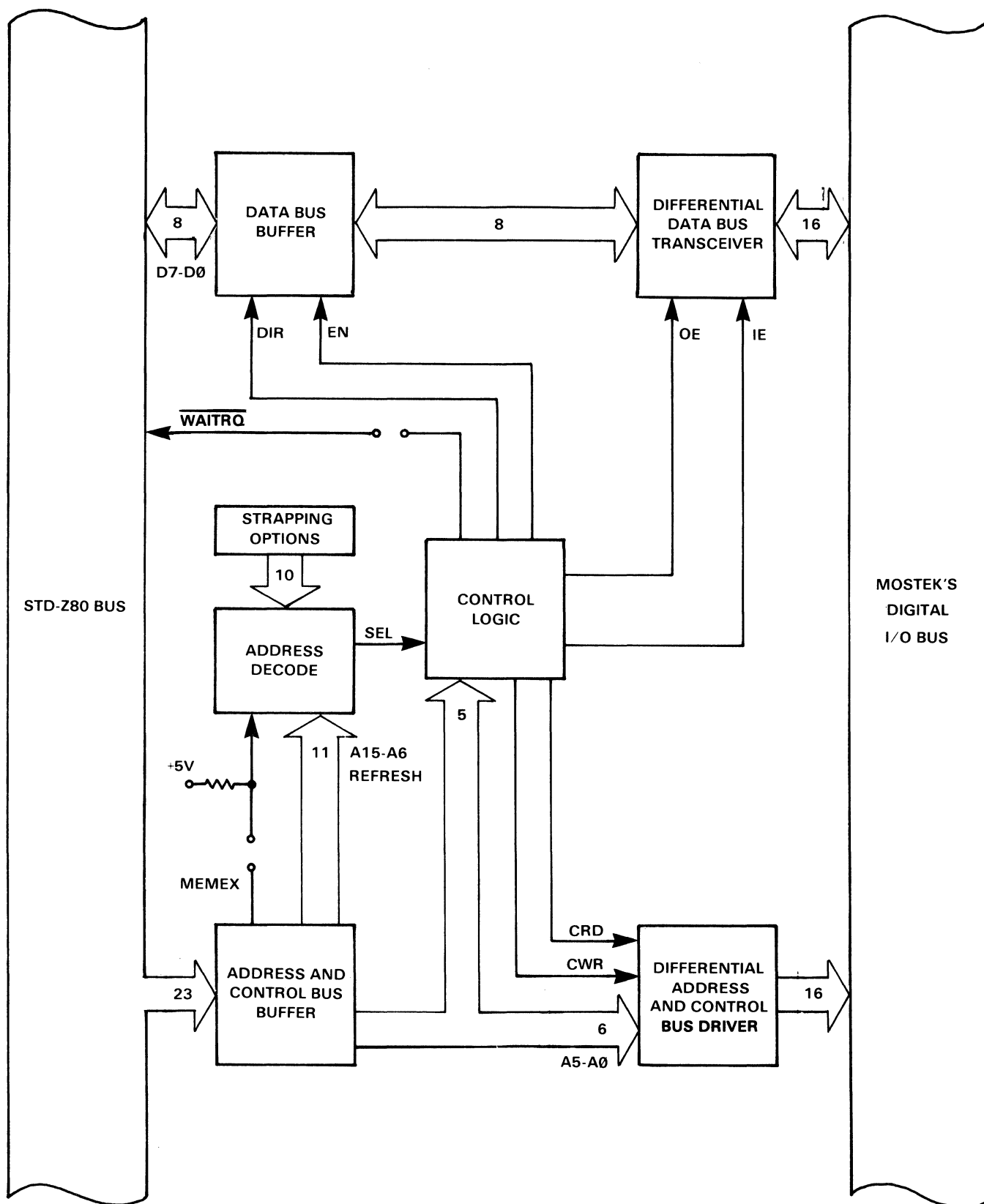


FIGURE 2-2 MDX-DIOB1 BLOCK DIAGRAM



SECTION 3

STRAPPING OPTIONS

3.1 ADDRESS CONFIGURATION STRAPPING

MDX-DIOB1 is address block selectable on 64 byte boundaries, providing maximum system flexibility. Address selection is done by matching the jumper plugs on J3 to the bit pattern for the desired address block. Inserting a jumper plug causes the corresponding address bit to be set low. A work sheet is provided in Figure 3-1. J3 is defined as follows:

TABLE 3-1 J3 HEADER PINOUT

PINS	ADDRESS BIT
1 - 2	A15
3 - 4	A14
5 - 6	A13
7 - 8	A12
9 - 10	A11
11 - 12	A10
13 - 14	A9
15 - 16	A8
17 - 18	A7
19 - 20	A6

3.2 MEMORY EXPANSION

A memory expansion option is provided on MDX-DIOB1 to allow compatibility with systems that use the /MEMEX signal on the STD BUS. When this option is used, the address decode circuit on MDX-DIOB1 will generate its address select signal only when /MEMEX is active low. This option can be omitted by not installing a jumper plug between pins 1 and 2 on J4.

3.3 ONE WAIT-STATE GENERATOR

This option is used with 4MHz systems when the DIGITAL I/O BUS length is greater than 25 feet. Otherwise, this option is not necessary and can be omitted by not installing a jumper between pins 3 and 4 on J4. The maximum recommended DIGITAL I/O BUS length for 2.5MHz or 4MHz operation is 50 feet.

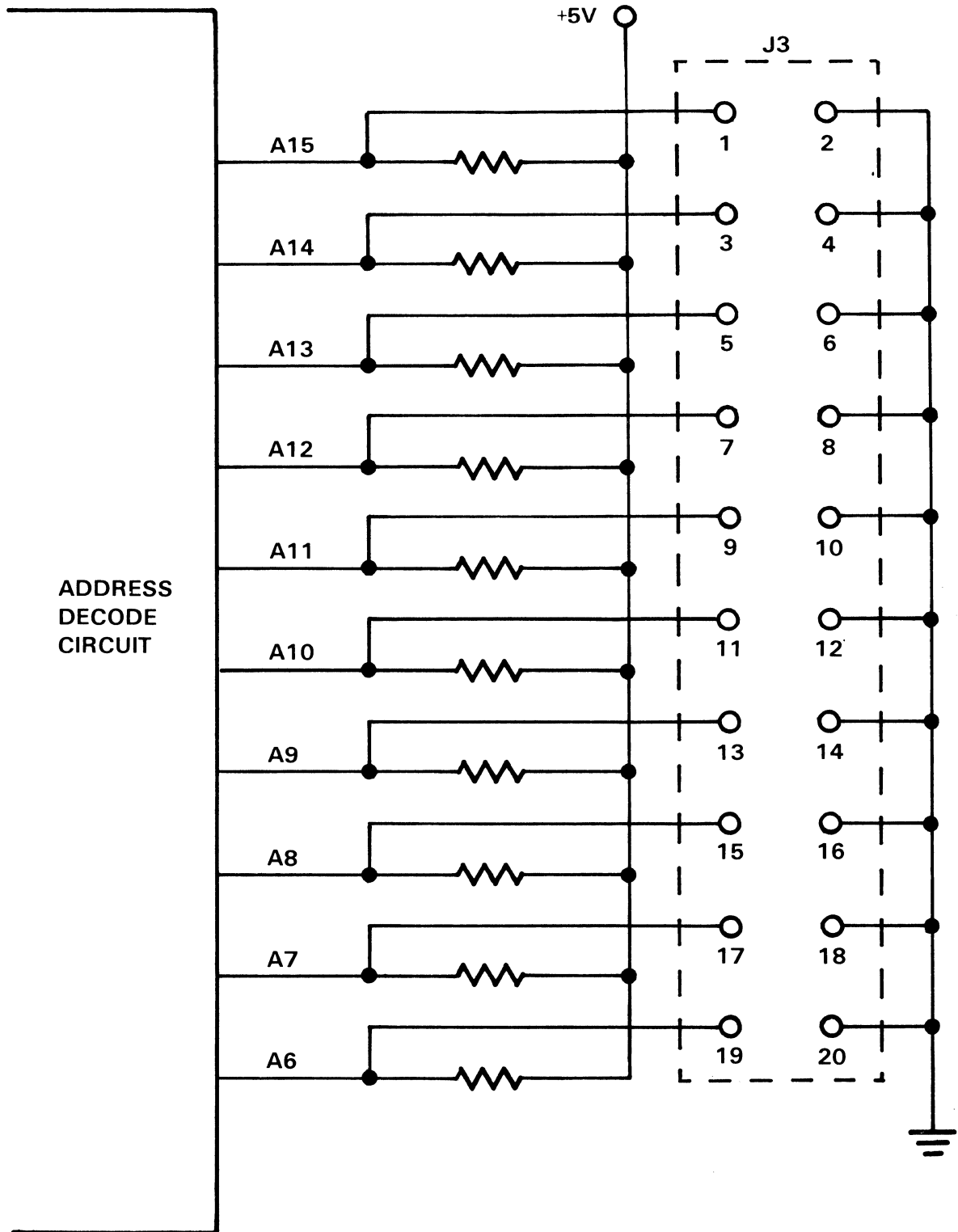
3.4 $\overline{\text{BUSAK}}$ TO $\overline{\text{STATUS } 0}$

This option is used to complete the priority daisy-chain when multiple DMAs are used in the system. Since multiple DMAs are not normally used in MOSTEK's MD systems, this option can be omitted by not installing a jumper between pins 5 and 6 on J4.

3.5 SHIPPING CONFIGURATION

All jumper locations are shipped open. A set of jumper plugs are supplied in a separate bag. A jumper option can be strapped using one of these jumper plugs or a wire-wrap connection.

FIGURE 3-1 ADDRESS STRAPPING OPTION WORK SHEET



SECTION 4

DIGITAL I/O BUS DESCRIPTION

4.1 INTRODUCTION

All DIGITAL I/O BUS lines are transmitted over balanced differential, twisted pair lines with provisions for termination resistors at each end of the bus. This method insures adequate noise immunity in industrial environments. A 40 pin latching type connector is used to provide positive locking to the DIGITAL I/O BUS. A 40 conductor twisted pair flat cable is used to interconnect DIGITAL I/O BUS peripherals (e.g., MOSTEK's DIOP) and MDX-DIOB1. Figures 4-1 and 4-2 show the typical configurations for signals found on the DIGITAL I/O BUS.

4.2 ADDRESS SIGNALS

A5-A0 constitute port address selection. Each DIGITAL I/O BUS peripheral compares these signals to its preset strapping options to generate its address enable and port select signals. A5-A0 are always enabled on the DIGITAL I/O BUS, which means a DIGITAL I/O BUS peripheral will receive a valid address even though MDX-DIOB1 is disabled. This is of no consequence, however, since the control signals generated by MDX-DIOB1 will be inactive.

4.3 CONTROL SIGNALS

CRD and CWR are coded control signals. On receipt of a CRD command, the port selected by A5-A0 will place its data on D7-D0 of the DIGITAL I/O BUS and hold it there until CRD is released. On receipt of a CWR command, the port selected by A5-A0 will capture the data on D7-D0 of the DIGITAL I/O BUS at the trailing edge of CWR. The coincidence of CRD and CWR both active constitutes a reset condition, which clears all DIGITAL I/O BUS output peripherals. CRD and CWR are always enabled on the bus and are inactive unless one of the following conditions exist:

- 1) MDX-DIOB1 is enabled.
- 2) SYSRESET is active.
- 3) DIGITAL I/O BUS is open-circuited.

The differential receivers incorporate a fail-safe operation which will activate their outputs whenever their inputs are open-circuited. Note that this occurrence generates a reset condition.

4.4 DATA SIGNALS

D7-D0 constitute the bidirectional data signals to and from all DIGITAL I/O BUS peripherals. These lines are arranged in a party line configuration on the DIGITAL I/O BUS and are always tri-stated unless MDX-DIOB1 is enabled.

4.5 ROUTING

The maximum recommended DIGITAL I/O BUS length for 2.5MHz operation is 50 feet, with or without the one wait-state generator option. For 4MHz operation, the maximum recommended length is 25 feet without the wait-state option, and 50 feet with the wait-state option. The 40 conductor twisted pair flat cable can be tapped in ten-inch intervals, and should be laid out in a point-to-point, daisy-chain fashion. Branching from the DIGITAL I/O BUS should be avoided. Termination resistors (100Ω, 16PIN DIP packages) should be located only on the end of the DIGITAL I/O BUS.

WARNING: If more than one DIGITAL I/O BUS peripheral contains termination resistors, damage to the bus drivers will result.

FIGURE 4-1 TYPICAL ADDRESS OR CONTROL LINE

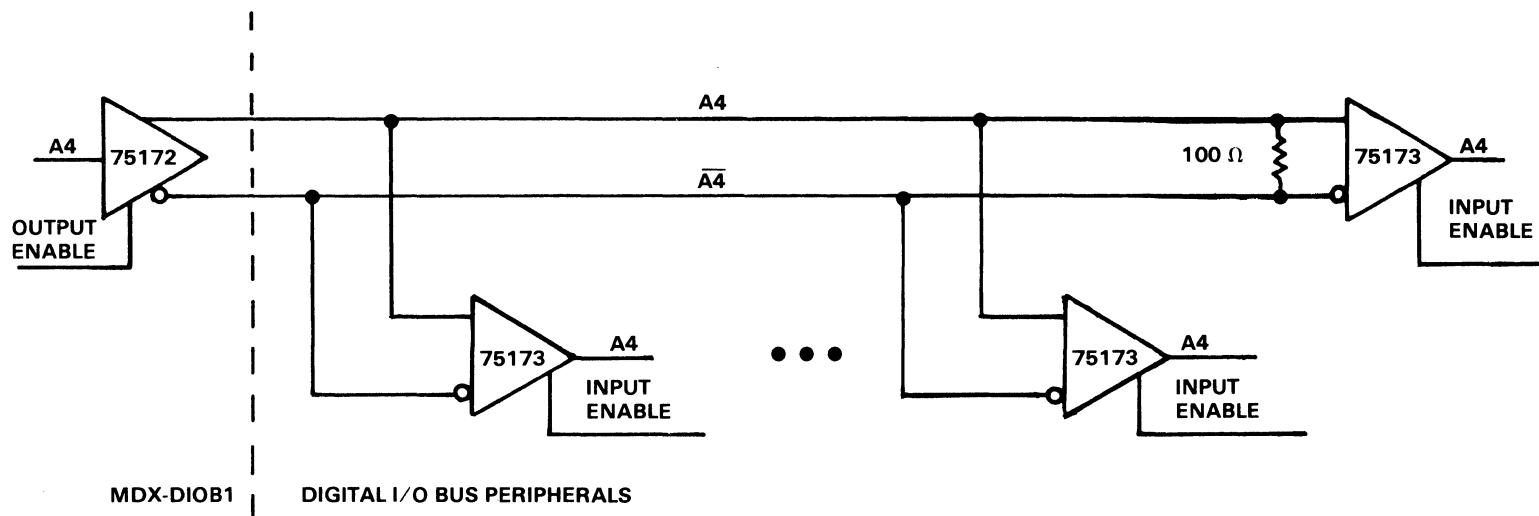
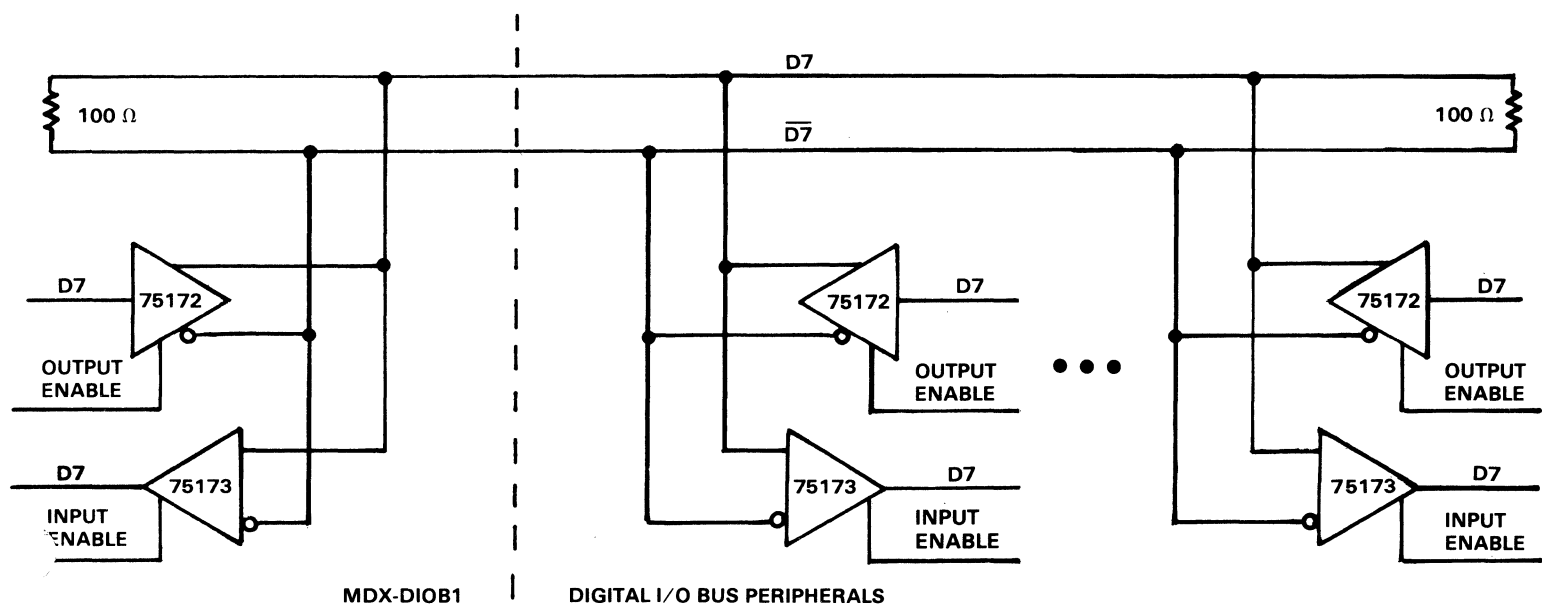


FIGURE 4-2 TYPICAL DATA LINE



SECTION 5

SPECIFICATIONS

5.1 ELECTRICAL SPECIFICATIONS

5.1.1 WORD SIZE

8 bits

5.1.2 BUS INTERFACE

STD-Z80 BUS

Inputs	One 74LS load maximum
Outputs	IOL = 24mA at 0.5V maximum
	IOH = -3mA at 2.4V minimum
	IOZL = -2000uA maximum at 0.4V
	IOZH = 20uA maximum at 2.7V

DIGITAL I/O BUS

Inputs	VTH = 0.2V maximum (differential input sensitivity)
	IIN = 1.0mA maximum
Outputs	IOL = 60mA at 1.1V maximum
	IOH = -60mA at 3.5V minimum
	IOZ = +1000uA maximum

5.1.3 POWER SUPPLY REQUIREMENTS

+5V +5% at 0.9A maximum

5.1.4 OPERATING TEMPERATURE RANGE

0°C to 60°C

5.1.5 INTERRUPTS

No interrupt capability.

5.1.6 I/O ADDRESSING

On board programmable on 64 byte boundaries.

5.1.7 I/O CAPACITY

Provides parallel, memory-mapped I/O to a maximum of sixty-four 8-bit ports, or 16 of Mostek's DIOPs

5.1.8 SYSTEM CLOCK

250KHz minimum

4.0MHz maximum

5.2 MECHANICAL SPECIFICATIONS

5.2.1 CARD DIMENSIONS

4.5 in. (11.43cm) high by 6.50 in. (16.51cm) long

0.675 in. (1.71cm) maximum profile thickness

0.062 in. (0.16cm) printed circuit board thickness

5.2.2 CONNECTORS

FUNCTIONS	CONFIGURATION	MATING CONNECTORS
STD-Z80 BUS	56 pin 0.125 in. centers	Printed Circuit Viking 3VH28/ICE5
		Wire Wrap Viking 3VH28/ICND5
		Solder Lug Viking 3VH28/ICN5

DIGITAL I/O BUS	Socket Connector 40 pin dual RA 0.100 in. centers	3M 6040 Ansley 609-4001M
-----------------	---	-----------------------------

APPENDIX A

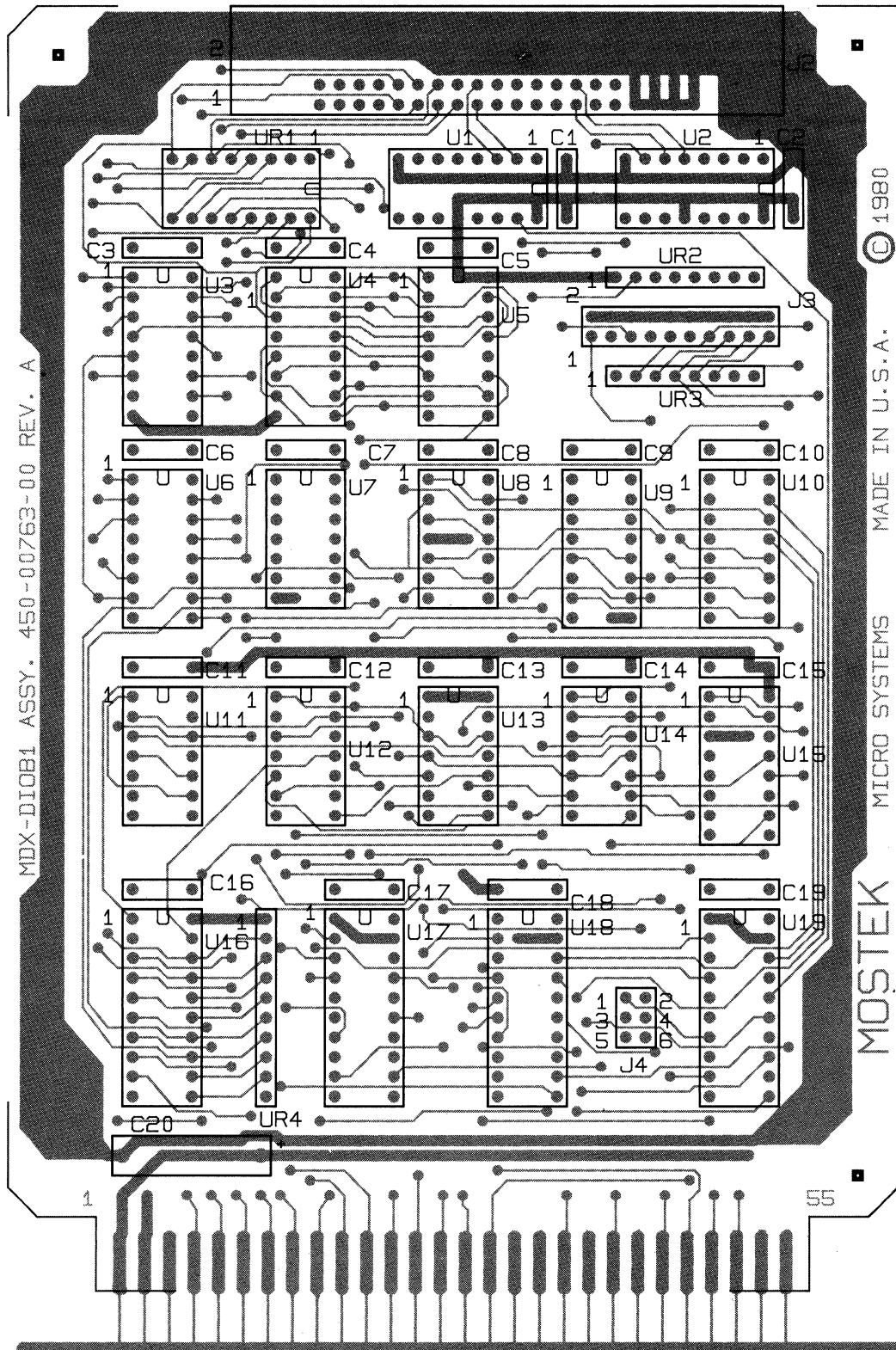
SCHEMATIC

APPENDIX B

PARTS PLACEMENT DIAGRAM

PARTS LIST

PARTS PLACEMENT DIAGRAM



[illegible]

MOSTEK®

1215 W. Crosby Rd. • Carrollton, Texas 75006 • 214/323-6000

In Europe, Contact: MOSTEK Brussels
150 Chaussee de la Hulpe, B1170, Belgium;
Telephone: 660.69.24

Mostek reserves the right to make changes in specifications at any time and without notice. The information furnished by Mostek in this publication is believed to be accurate and reliable. However, no responsibility is assumed by Mostek for its use; nor for any infringements of patents or other rights of third parties resulting from its use. No license is granted under any patents or patent rights of Mostek.

PRINTED IN USA September 1980
Publication No. MK79861

Copyright 1980 by Mostek Corporation
All rights Reserved